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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,853	05/25/2001	Akihiko Ito	109158	4755

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EXAMINER	
ABDULSELAM, ABBAS I	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/856,853	ITO, AKIHIKO	
	Examiner	Art Unit	
	Abbas I Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-28,30-32,34-41,45 and 46* is/are rejected.

7)☒ Claim(s) *29,33 and 42-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *19*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see # 18, filed on 08/12/04, with respect to the rejection(s)of claim(s) 24-46 under U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Furuhashi et al. (USPN 5633659).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24-28, 30-32 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scheffer et al. (USPN 5852429) in view of Tsuchida et al. (USPN 6232938) and Furuhashi et al. (USPN 5633659).

Regarding claims 24 and 30, Scheffer teaches LCD matrix display system (10) including pixels (26) and a frame period (T). See Fig 1. Scheffer teaches gray scale method of addressing display (12) including a pulse width modulation where several frame periods T of the display information are used to control the duration of the time that the pixel is "on" compared with the time the pixel is "off" (col. 25, 18-23 and 39-44). Scheffer, in connection to pulse width modulation, teaches the time "on" and "off" information state of a pixel with respect to each time

interval delta (t) sub k being subdivided into G smaller time intervals delta (t) sub kg (col. 25, lines 45-67.) see Fig. 20. Furthermore, Scheffer teaches that electrode pattern as shown in Fig 1 comprises multiple rows and columns from which a pixel is formed at the intersection (col. 5, lines 38-43). Scheffer further teaches mathematical equations to calculate the use voltage across the pixel. For example, Scheffer teaches averaging the pixel voltage over a frame period, calculating ratio of the magnitude of the peak voltage occurring a given state of the pixel, and illustrating the "on" and "off" states of pixel with respect to "on" and "off" RMS voltage across the pixel. See col. 6, lines 55-67 (equations 5& 6), and col. 14,lines 21-46 (equations 37 and 38).

Scheffer does not teach "turning on of off pixel by applying to the pixel a one of two-level signals for a period of sub-field, the cumulation of on periods during the first time period of the single frame being variably controlled in accordance with a gray-scale level of the pixel for the gray-scale display".

Tsuchida et al. (USPN 6232938) on the other hand teaches are graphs (Fig 17A-F) showing examples of profiles of Output Enable (OE) that is supplied from the controller (33) to the address drivers 31U, 31M, and 31D of the liquid crystal cells. Tsuchida teaches a controller (33) supplies control signals, including clock signals and data signals, to the address drivers 31U, 31M, and 31D and data drivers 32U, 32M, and 32D. Tsuchida also teaches the controller (33) controls Output Enable (OE) of the address driving circuits 31U, 31M, and 31D so that one of three pixels on the three layers that compose one picture element is always selected at each of T1, T2, and T3 and that the sum of the elapsed time after the data write point or the sum of the fluctuation of the holding voltage levels after the data write point becomes almost equal in each picture element. Tsuchida illustrates for example, at t=T2, the controller 33 supplies Output

Enable (OE) to relevant address drivers so that the first sub-field of the liquid crystal cell 23 (the address lines GD1, GD4, and GD (3k-2)), the second sub-field of the liquid crystal cell 21 (the address lines GU2, GU5, and GU (3k-1)), and the third sub-field of the liquid crystal cell 22 (address lines GM3, GM6, and GM (3k)) are selected. See col. 15, lines 4-13 and Figs. 12-17.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Scheffer's display system to incorporate Tsuchida's controller (33) as configured in Fig. 16, and as implemented and demonstrated in Fig. 17. One would have been motivated in view of the suggestion in Tsuchida that use of the controller (33) equivalently provides the turning "on" & "off" each pixel in a desired fashion as well as the desired "accumulation of on periods". The use of the controller helps function a liquid crystal display device as taught by Tsuchida. However, Scheffer does not disclose turning "on' the pixels in the second time period in accordance with a threshold voltage of a transmissivity characteristics relative to a voltage applied to electro-optical material used in the electro-optical device. Furuhashi on the other and teaches a threshold voltage (801) generator which generates a threshold voltage for comparison with a detected voltage pulse transferred on the signal line 105. Furuhashi teaches a voltage comparator (802) for comparing the detected voltage pulse with the threshold voltage, and a determination circuit (803) for determining whether or not the detected voltage pulse is active according to the result of the voltage comparator (802). See Fig. 3. Furuhashi further teaches as shown in FIG. 31 is a timing chart showing the X-electrode voltage detection timing in the display.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Scheffer's display system to adapt Furuhashi's voltage correction

circuit including a threshold voltage (801) generator as shown in Fig. 3. One would have been motivated in view of the suggestion in Furuhashi that the voltage correction circuit as configured in Fig. 3 equivalently yields the voltage needed for the pixels in a the desired fashion. The use of voltage correction circuit helps function helps function a display unit as taught by Furuhashi.

Regarding claim 25, Furuhashi teaches that when the pen point 601 of the pen shown in FIG. 2 comes into contact with the liquid crystal panel 101, the spring 605 is pressed, causing the switch 602 to be turned on for transferring a GND level voltage, via the signal line 603, to the detected voltage correction circuit (106 in FIG. 1).

Regarding claims 27-28, 32, and 34, Scheffer teaches a display matrix (12) along with column and row signal generators and a swift function generator (96), which provides sequential swift function vector to row driver, IC 98. See col. 19, lines 1-14 and Fig 12. In addition, Scheffer teaches row and column addressing signals applied to LCD matrix including "on" and "off" states of pixel with respect to a period T. See Fig 1. In addition, Scheffer discloses a gray scale system using a technique of pulse width modulation in which the information state of a pixel is either "on" or "off". See col. 25, lines 39-48 and Fig. 20.

Regarding claim 35, Scheffer teaches matrix-addressing techniques inducing no frame response such as allowing only one "off" pixel per column. See col. 2, lines 56-63.

3. Claims 36-41 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. (USPN 5892495) in view of Scheffer et al. (USPN 5852429), Furuhashi et al. (USPN 5633659) and Tsuchida et al. (USPN 6232938).

Regarding claims 36, 38-39 and 41, Sakai teaches a matrix crystal type liquid crystal display panel (1) including multiple data lines (DL), multiple scanning lines (SL), a data line driving circuit (2), a scanning line driving circuit (3) and pixel (5) composed of a switching element (SW). Sakai teaches that the data line (DL) and the electrode of the pixel capacitor Cp, that is, a pixel electrode Ep are connected with the switching element SW. Sakai teaches that the scanning line driving circuit (3) sequentially selects the scanning lines (SL) and controls the closing and opening of the respective switching elements (SW) in the pixels (col. 9, lines 20-56 and Fig 2(a)). In addition, Sakai teaches the switching element for outputting the picture signal supplied from data lines to the pixel electrodes in accordance with the selection signal supplied to the scanning lines (col. 7, lines 65-67, col. 8, lines 1-4). Sakai teaches the scanning circuit with respect to a period of time required for sampling the picture as well as the data line driving circuit (2) sequentially selecting the picture signals inputted during a period of a predetermined duration and supplies signals to the data lines (col. 6, lines 52-62 and col. 9, lines 54-56).

However, Sakai does not teach the scanning line with respect to a single frame time and sub-fields. Sakai also does not teach a data line-driving circuit with respect to signals "each designating turning on or off each pixel in accordance with a gray-scale level of respective pixels. Scheffer as discussed above teaches the time "on" and "off" information state of a pixel with respect to each time interval delta (t) sub k being subdivided into G smaller time intervals delta (t) sub kg (co. 25, lines 45-67 and Fig 7, Fig 20). Scheffer also teaches the use of a frame period (T) with respect to row and column signals of the LCD display (12) (col. 5, lines 12-24 and 50-53).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Sakai's display system to include Scheffer's frame and pulse width modulation technique that is used to control the state of pixels (26). One would have been motivated in view of the suggestion in Scheffer that frame and pulse width modulation technique equivalently provides the desired frame time along with the state of pixels (on and off). The use of frame and pulse width modulations helps function LCD display panel as taught by Scheffer.

Sakai has been described above. However, Sakai does not disclose "turning on or off pixels in accordance with a threshold value of a transmissivity characteristics relative to a voltage applied". Furuhashi on the other and teaches a threshold voltage (801) generator which generates a threshold voltage for comparison with a detected voltage pulse transferred on the signal line 105. Furuhashi teaches a voltage comparator (802) for comparing the detected voltage pulse with the threshold voltage, and a determination circuit (803) for determining whether or not the detected voltage pulse is active according to the result of the voltage comparator (802). See Fig. 3. Furuhashi further teaches as shown in FIG. 31 is a timing chart showing the X-electrode voltage detection timing in the display.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sakai's display system to adapt Furuhashi's voltage correction circuit including a threshold voltage (801) generator as shown in Fig. 3. One would have been motivated in view of the suggestion in Furuhashi that the voltage correction circuit as configured in Fig. 3 equivalently yields the voltage needed for the pixels in a the desired fashion. The use of voltage correction circuit helps function helps function a display unit as taught by Furuhashi.

Sakai does not teach "turning on of off pixel by applying to the pixel a one of two-level signals for a period of sub-field, the cumulation of on periods during the first time period of the single frame being variably controlled in accordance with a gray-scale level of the pixel for the gray-scale display".

Tsuchida et al. on the other hand teaches are graphs (Fig 17A-F) showing examples of profiles of Output Enable (OE) that is supplied from the controller (33) to the address drivers 31U, 31M, and 31D of the liquid crystal cells. Tsuchida teaches a controller (33) supplies control signals, including clock signals and data signals, to the address drivers 31U, 31M, and 31D and data drivers 32U, 32M, and 32D. Tsuchida also teaches the controller (33) controls Output Enable (OE) of the address driving circuits 31U, 31M, and 31D so that one of three pixels on the three layers that compose one picture element is always selected at each of T1, T2, and T3 and that the sum of the elapsed time after the data write point or the sum of the fluctuation of the holding voltage levels after the data write point becomes almost equal in each picture element. Tsuchida illustrates for example, at t=T2, the controller 33 supplies Output Enable (OE) to relevant address drivers so that the first sub-field of the liquid crystal cell 23 (the address lines GD1, GD4, and GD (3k-2)), the second sub-field of the liquid crystal cell 21 (the address lines GU2, GU5, and GU (3k-1)), and the third sub-field of the liquid crystal cell 22 (address lines GM3, GM6, and GM (3k)) are selected. See col. 15, lines 4-13 and Figs. 12-17.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sakai's display system to incorporate Tsuchida's controller (33) as configured in Fig. 16, and as implemented and demonstrated in Fig. 17. One would have been motivated in view of the suggestion in Tsuchida that use of the controller (33) equivalently

provides the turning "on" & "off" each pixel in a desired fashion as well as the desired "accumulation of on periods". The use of the controller helps function a liquid crystal display device as taught by Tsuchida.

Regarding claims 37 and 40, Sakai teaches an address signal with respect frequencies and time required for reading data corresponding to each pixel. See col. 6, lines 25-34.

Regarding claims 45-46, Sakai teaches a display system where in the pixel electrodes, the elements, and the data line driving circuit are provided on either amorphous silicon thin film or monocrystalline silicon film formed on insulating substrate. See col. 8, lines 5-9.

Allowable Subject Matter

4. Claims 29, 33 and 42-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Abbas Abdulselam** whose telephone number is **(703) 305-8591.** The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard Hjerpe**, can be reached at **(703) 305-4709.**

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

January 5, 2005

XIAO WU
PRIMARY EXAMINER